REMARKS

This amendment is responsive to the Office Action mailed January 30, 2003. Claims 1-3 and 6-18 are currently pending in the application. Claims 19-29 are withdrawn from consideration in response to the telephonic negotiation with the Examiner on January 6, 2003, concerning the issuance of a Restriction Requirement. This amendment amends Claims 1, 2, 3, and 8 to clarify the claimed subject matter to allow one skilled in the art to more fully appreciate Applicants' claimed invention. This amendment also cancels Claims 4 and 5 without prejudice. The amendments present no new matter and they present no new issues and hence, require no further search. The amendments to Claims 1, 2, 3, and 8 are drafted to expressly clarify the claimed subject matter and are not directed to any art rejection. Accordingly, we understand that any further rejection of any of Claims 1-3 and 6-18 based on new art is to be non-final.

In view of the amendments made above and the comments set forth below, Applicants' respectfully urge the Examiner to reconsider the outstanding rejection and pass the claims to allowance.

Attached hereto is a marked-up version of the changes made to the claims, the abstract, and the specification by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made**".

Restriction Requirement:

With regard to Applicants' provisional election made with traverse on January 6, 2003 to prosecute the invention of Group I, Claims 1-18, Applicant now elects the claims of Group I, namely Claims 1-18 without traverse. Thus, Claims 19-29 are withdrawn from further consideration as a result of the selection without prejudice to Applicants' filing one or more divisional applications.

Drawings:

With regard to the Examiner's rejection to the drawing under 37 C.F.R. § 1.83(a) Applicants' amend Claims 1 and 2 to clarify that the claimed input/output interface

includes an input node and output node as illustrated in Figure 1. Figure 2 is amended to identify waveform 30 as an input waveform and to identify waveform 32 as an output waveform, further clarifying the subject matter recited in Claims 1-3 and 6-18.

Concerning the Examiner's objection to the drawing for failing to show "an interface" Applicants' direct the Examiner to Figure 1 specifically input node 18 and output node 16 and further to the specification on page 6, lines 17-22 and amended Claim 1.

With regard to the Examiner's objection to the drawings concerning "clock cycle of clock signal asserted on the clock input node 24", "a fixed number of clock cycles on the clock input node 24", and "relation of clock cycle with input/output signal and register as described in the specification". Applicants' contend that the skilled practitioner in the electrical arts readily understands and comprehends that an interface includes one or more input and output nodes and further comprehends without need for illustration the function and operation of a clock signal asserted on a clock input node and a relationship between a clock signal and the input waveform 30 and the output waveform 32 as described in detail throughout the specification. Thus, Applicants' consider the clock feature of the present invention as a conventional feature found on almost every integrated circuit and is sufficiently described in the specification with regard to the input waveform 30 and the output waveform 32 so that detailed illustration is not essential for a proper understanding of the invention. Accordingly, Applicants' invention is properly illustrated in the drawings in the form of a graphical symbol or labeled representation i.e. clock 24 in Figure 1 as required by 37 C.F.R. § 1.83(a). Hence, Applicant contends that no further drawing amendments are needed because the drawings as amended comply with 37 C.F.R. § 1.83. Accordingly, Applicants' request the Examiner to reconsider and withdraw his objection to the drawings.

Specification:

Applicant amends the specification to correct the informalities identified by the Examiner.

Regarding the Examiner's objection of the disclosure under 37 C.F.R. § 1.71, Applicants' contend that the specification as filed complies with 37 C.F.R. § 1.71. The

specification as filed includes a written description of the invention and includes a written description of the manner and process of making and using the same. The specification is written in full, clear, concise, and exact terms so as to enable any person skilled in the arts relating to the claimed invention to make and use the same without undue experimentation.

To address the Examiner's informalities concerns, the specification on page 6, line 20 is amended to indicate that the output node 16 is adapted to communicate a digital signal that includes at least three values. Furthermore, the specification on page 7 is amended to illustrate that the input signal 30 is asserted on the input node 18 and the output signal 32 is communicated from the output node 16. No new matter is added by these amendments.

Concerning the Examiner's comments on the first, second, and third value recited throughout the specification, Applicants' fail to comprehend the Examiner's comments "not compared with other signal of drawing, why?" and request clarification. Applicants' failure to comprehend Examiner's comment is due in part that one skilled in the art would readily recognize that the two waveforms illustrated correspond to an input waveform and an output waveform that may or may not have a phased relationship. Applicants' contend that those skilled in the art will readily recognize that an input signal or trigger to trigger an event or occurrence often occurs before an output is generated and the output signal is asserted, if at all, at some time in the future. Thus, it is not necessary to compare the graphical representation of output signal 32 with the graphical representation of input signal 30, or to a clear signal, as suggested by the Examiner. Accordingly, Applicants' respectfully urge the Examiner to reconsider and withdraw the objection to the specification under 37 C.F.R. § 1.71.

Abstract:

With regard to the Examiner's objection to the abstract, an amended abstract is provided.

Claim Rejections under 35 U.S.C. § 112:

Claims 1-10 stand rejected under 35 U.S.C. § 112, first paragraph, for allegedly containing subject matter which is not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventors at the time that the application was filed had possession of the claimed invention. Applicants' respectfully traverse this rejection on the basis of the following arguments, and further contend that the specification as originally filed reasonably conveys to the skilled artisan in the relevant art that the inventors at the time the application was filed had possession of the claimed invention.

Regarding the rejection of Claim 1, the Examiner is respectfully directed to Figure 2, namely output signal 32 and throughout the specification wherever output signal 32 is described in support of the indicative feature recited in Claim 1, for example, page 8, lines 7-12 of the specification.

Concerning the rejections of Claim 2 the Examiner is directed to the specification on page 7, lines 10 and 11.

Concerning the Examiner's rejection of Claim 6 and 7 the Examiner is respectfully directed to the background of the invention portion of the specification as well as to the summary of the invention portion of the specification.

Concerning the Examiner's rejection of Claim 9 Applicants' respectfully direct the Examiner's attention to the specification namely, page 6, line 13.

Regarding the Examiner's rejection of Claim 10, Applicants' respectfully direct the Examiner to the summary of the invention portion of the specification.

Regarding the rejection of Claim 3, Applicants' direct the Examiner to Figure 2, namely output signal 32 and to the specification wherever output signal 32 is described in

detail to support the indicative feature recited in Claim 1, for example page 8, lines 7-12 of the specification.

Regarding the rejections of Claim 4 and 5, Applicants' consider this rejection moot for Claims 4 and 5 are cancelled without prejudice.

Concerning the rejection of Claim 8, the Examiner is respectfully directed to Figure 2, namely output signal 32 and throughout the specification wherever output signal 32 is described to support the indicative feature recited in Claim 1, for example, page 8, lines 7-12 of the specification.

Concerning the rejection of Claim 17, Applicants' direct the Examiner's attention to the summary of the invention section of the specification.

Concerning the rejection of Claim 18, Applicants' respectfully direct the Examiner's attention to the summary of invention portion of the specification.

In summary, the Examiner has failed his initial burden of presenting by a preponderance of evidence why a person skilled in the art would not recognize an Applicants' disclosure a description of the invention recited by the claims. The description as filed is presumed to be adequate, and in fact is adequate. The Examiner has failed to offer sufficient evidence or reasoning to detract or rebut the presumption of adequacy. Accordingly, Applicants' request the Examiner to reconsider and withdraw the claim rejections under 35 U.S.C. § 112, first paragraph.

Claims Rejections under 35 U.S.C. § 112, second paragraph:

Claims 11-18 stand rejected under 35 U.S.C. § 112, second paragraph for allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants' regard as their invention.

Claims 11-18 properly set forth the subject matter that Applicants' regard as their invention and recite with clarity and particularity to distinctly define the subject matter of Applicants' invention. That is, contrary to the Examiner's assertion, Applicants' invention at the completion of a step of sensing by a thermal sensor a temperature of an integrated circuit asserts an output signal on a second input/output pin of the thermal sensor by the thermal sensor. The output signal provides the temperature of the integrated circuit and provides an indication that the thermal sensor is functioning properly. The Examiner contends that "completion of said step of sensing" is not clear, because there is no indication of how and when sensing is complete. Applicants' contend that the scope of Claim 11 is clear to one skilled in the art. That is, in the method recited in Claim 11 the output signal is asserted after completion of the step of sensing by said thermal sensor a temperature of the integrated circuit. Claim 11 does not recite a limitation that requires an empirical indication (i.e. x seconds) of "how and when sensing is completed" nor is such a limitation a requirement of U.S. Patent Law or for one skilled in the art to readily understand the scope of Applicants' invention. The language of Claim 11 as filed is clear, concise and definite. Accordingly, Applicants respectfully urge the Examiner to reconsider and withdraw the rejection of Claims 11-18 under 35 U.S.C. § 112, second paragraph.

Claim Rejections under 35 U.S.C. § 103

For purposes of clarity in the discussion below, the respective claim rejections under 35 U.S.C. § 103, are discussed separately.

A. Rejection of Claims 1-10 under 35 U.S.C § 103(a):

The Office Action rejects Claims 1-10 as being unpatentable over U.S. Patent No. 6,091,255 of Godfrey (hereinafter "Godfrey"). Applicants' respectfully traverse this rejection on the basis of the following arguments, and further contend that Godfrey fails to teach or suggest all elements of these claims, as described below, and hence, does not anticipate the claimed invention.

Summary of the Claimed Invention:

Applicants' invention recited in Claims 1-10 is directed to a thermal sensor in an integrated circuit. The thermal sensor includes a register and an input/output interface. The register holds a response of the thermal sensor and the input/output interface includes an input node to receive an input trigger to trigger the thermal sensor to output on an output node of the interface an output signal. The output signal includes the response held by the register, an indicator that indicates the thermal sensor is sensing the temperature of the integrated circuit and a value generated by the thermal sensor that indicates the thermal sensor is functioning properly.

An advantage of the thermal sensor for sensing a temperature of an integrated circuit of the present invention is the simplicity of construction, conservation of costs and the ease in utility of the thermal sensor and method. The sensor and method benefit an integrated circuit that seeks a sensor capable of indicating its operability while keeping the external pin density of the integrated circuit to a minimum. As a result, an integrated circuit can communicate an accurate internal temperature reading from an internal sensor to a device external to the integrated circuit and provide an indication of the sensors operability as part of the communication without significantly increasing external pin density of the packaged integrated circuit.

Claims 1-3 And 6-10 Are Patentably Distinct From The Godfrey Patent:

Claims 4 and 5 are cancelled by this amendment and therefore the rejection of Claims 4 and 5 are moot.

The Godfrey Patent is directed to an on chip thermometer having a clock circuit, a temperature responsive circuit or thermal sensor, and a counter. The clock circuit operates at a fixed frequency and generates a clock signal at the fixed frequency. The temperature responsive circuit or temperature sensor couples to the clock circuit and receives the clock signal from the clock circuit. In response to receiving an enable signal, the temperature responsive circuit or temperature sensor generates an output signal. The counter is coupled to receive the output signal from the temperature responsive circuit.

The counter than generates the value indicative of a local temperature of the integrated circuit. The thermometer optionally includes a register electronically coupled to the counter, physically located outside of the temperature responsive circuit or temperature sensor.

Claims 1-3 and 6-10 are not rendered unpatentable by Godfrey. Godfrey fails to teach or disclose each and every element recited in Claim 1-3 and 6-10. Specifically, Godfrey fails to teach or suggest a thermal sensor in an integrated circuit that includes a register and an input/output interface, having an input node to receive an input trigger to trigger the thermal sensor to output on an output node of the interface an output signal. Furthermore, Godfrey fails to teach or suggest that the output signal from the thermal sensor includes a response held by the register, an *indicator* that indicates the thermal sensor is sensing the temperature of the integrated circuit and a *value* generated by the thermal sensor that indicates the thermal sensor is functioning properly. Nowhere does Godfrey teach or suggest a thermal sensor that includes an input/output interface having an input node to receive an input trigger to trigger the thermal sensor to output on an output node of the interface an output signal that includes the response held by the register, an indicator that indicates the thermal sensor is sensing the temperature of the integrated circuit and a valued generated by the thermal sensor that indicates that the thermal sensor is functioning properly.

The Examiner cites Figures 1-6 and column 3, lines 41-56 of Godfrey as teaching or suggesting a thermal sensor that includes a register to hold a response of the thermal sensor. Moreover, the Examiner cites Figures 1-6 and column 3, lines 41-56 as teaching or suggesting the input/output interface of Applicants' thermal sensor that includes an input node to receive an input trigger to trigger the thermal sensor to output on an output node of the interface an output signal that includes the response held by the register, an indicator that indicates the thermal sensor is sensing the temperature of the integrated circuit and a value generated by the thermal sensor that indicates the thermal sensor is functioning properly. The Applicants' respectfully submit that the passages and figures cited by the Examiner merely teach or suggest a thermometer that includes a clock

circuit, a temperature responsive circuit or temperature sensor, a counter and a register coupled to the counter, not a thermal sensor that includes an interface for asserting an output signal that includes a response held by the register, an indicator that indicates the thermal sensor is sensing, and a value generated by the thermal sensor that indicates the thermal sensor to functioning property.

The Godfrey patent merely discloses a thermometer that includes a number of circuits including a clock circuit, a temperature responsive circuit or temperature sensor, a counter, and optionally a register coupled solely to the counter. Moreover, the Examiner admits that Godfrey fails to teach or disclose a thermal sensor having an input/output interface that outputs an output signal on an output node that includes a value generated by a thermal sensor that indicates the thermal sensor is functioning properly. Furthermore, the Examiner merely makes a conclusory statement that it would have been obvious to one skilled in the art at the time the invention was made that a sensor outputting a signal after triggered by a trigger signal that it is proper to understand the sensor is functioning properly. Contrary to the Examiner's assertion, Godfrey merely asserts an output signal having a value that indicates a temperature of the integrated circuit. The output signal from the thermometer disclosed by Godfrey fails to include an indication that the sensor is sensing and fails to include a value that indicates whether the thermal sensor is operating properly. One skilled in the art readily recognizes that merely because a device is outputting a signal after being triggered by a trigger signal is not clear and definite indication that the device is functioning properly.

Hence, Applicants' contend that Godfrey fails to teach or suggest each and every feature recited in Claims 1-3 and 6-10. Moreover, Applicants' contend that the Examiner fails to provide a motivation or suggestion, other than from Applicants' own invention, that a thermal sensor include a register and further output an output signal in response to an input signal that provides a temperature value, an indication that the sensor is sensing and a value that indicates the sensor is functioning properly. As a result, the Examiner fails to establish a *prima facie* case of obviousness. Accordingly, Applicants' request the

Examiner to reconsider and withdraw the rejection of Claims 1-3 and 6-10 under 35 U.S.C. § 103(a).

B. Rejection of Claims 11-18 under 35 U.S.C. § 103(a):

Claims 11-18 are directed to a method for a thermal sensor in an integrated circuit to provide an indication that the thermal sensor is functioning properly. The use if the thermal sensor enables other integrated circuits to receive the response from the integrated circuit having a thermal sensor and determine from the response of the thermal sensor whether the thermal sensor is functioning properly. In accordance with the method of Claims 11-18, an input signal is asserted on a first input/output pin of the thermal sensor to initiate thermal sensing of the integrated circuit by the thermal sensor. In turn, the thermal sensor senses a temperature of the integrated circuit. At completion of the step of sensing, the thermal sensor asserts an output signal on a second input/output pin of the thermal sensor. The output signal provides the temperature of the integrated circuit and provides an indication that the thermal sensor is functioning properly.

Godfrey is concerned with a thermometer that includes a temperature sensor and is not concerned with a method for a thermal sensor to provide an indication that the thermal sensor is functioning properly. Nowhere does Godfrey teach or suggest that the output signal from the temperature sensor of the thermometer includes an indication that the sensor is functioning properly. Moreover, as discussed above, the Examiner's conclusory statements fails to provide a suggestion or motivation to one skilled in the art to modify Godfrey to provide an output signal that includes a temperature of the integrated circuit and an indication that the thermal sensor is functioning properly.

Thus, Applicants' contend that Godfrey fails to teach or suggest each and every feature recited in Claims 11-18. Furthermore, Applicants' contend that neither the Examiner nor the Godfrey reference provides a suggestion or motivation to modify the Godfrey reference. As a result, the Examiner fails to establish a *prima facie* case of obviousness. Accordingly, Applicants' urge the Examiner to reconsider and withdraw the rejection of Claims 11-18 under 35 U.S.C. § 103(a).

CONCLUSION

In view of the amendments and remarks set forth above, Applicants' contend that Claims 1-3 and 6-18 are presently pending in this application, are patentable and in condition for allowance. If the Examiner deems there are any remaining issues, we invite the Examiner to call the undersigned at (617) 227-7400.

Respectfully submitted,

LAHIVE & COCKFIELD, LLP

David R. Burns
Registration No. 46,590
Attorney for Applicants

28 State Street
Boston, MA 02109
(617) 227-7400
(617) 742-4214
Dated: March 20, 2003

VERSION WITH MARKING TO SHOW CHANGES MADE

In the Abstract:

Please replace the abstract of the invention with the following rewritten abstract:

[An apparatus] A sensor and method are provided for sensing a physical stimulus in an integrated amount, such as thermal energy and produce a signal that indicates a quantitative value of the physical stimulus along with a value that indicates the operability of the [apparatus] sensor and a value that indicates a sense operation is in process. The [apparatus] sensor and method minimize the number of input and output pins necessary for [an apparatus] a sensor to report a measurement response of a physical stimulus.

In the Specification:

Please amend page 5, paragraph 4 to page 7 paragraph 2 as follows:

Figure 1 is a block diagram of an exemplary integrated circuit 12 that is suitable for practicing the illustrative embodiment of the present invention. The sensor 14 is an active device within the exemplary integrated circuit 12. The sensor 14 includes a register 15 to hold a response to a physical stimulus. Coupled to the sensor 14 are the clock input node 24, the power input node 22, the ground node 20, the input node 18 and the output node 16. Input node 18 and output node 16 provide the sensor 14 with an interface external to the exemplary integrated circuit 12. The power input node 22 is tied to a voltage source that can be controlled independently of the voltage source supplying a voltage level to the remainder of the active devices within the exemplary integrated circuit 12. The clock node 24 is also coupled to a clock source or driver that can be

controlled independently of any other clock source driver within the exemplary integrated circuit 12. As a consequence, the sensor 14 can be operated independently of the exemplary integrated circuit 12 and therefore used to determine a base line temperature of the exemplary integrated circuit 12 for calibration purposes. In this manner, the sensor 14 can be calibrated without having to compensate for the thermal affects of having one or more other active elements within the exemplary integrated circuit 12 active during baselining.

The input node 18 is adapted to receive a digital input signal that triggers the sensor 14 to sense a physical stimulus and report a response corresponding to an absolute or relative value of the physical stimulus. The output node 16 is adapted to communicate a digital signal that includes at least three values to indicate [indicates] that the sensor 14 is in process of sensing a physical stimulus, the response held by the register 15 along with a data value that indicates whether the sensor 14 is functioning correctly. The operation of the input node 18 and the output node 16 are discussed in more detail [above] with reference to Figures 2 and 3.

Those of ordinary skill in the art will recognize that power input node 22 and the clock input node 24 can also be coupled to a common clock node and a common power node within the integrated circuit 12 should a baseline temperature measurement with all operating elements in an off state not be necessary. The ground node 20 typically shares a common ground plane with the exemplary integrated circuit 12. Moreover, those skilled in the art will recognize that the input node 18 and the output node 16 can be

adapted to provide the sensor 14 with an interface internal to the exemplary integrated circuit 12.

Figure 2 is a waveform diagram that illustrates the digital signals communicated to the input node 18 and from the output node 16. The input signal 30 asserted on the input node 18 acts as a reset signal to reset the sensor 14 and initiate a sensing operation by the sensor 14. The output signal 32 communicated from the output node 16 is a digital signal that toggles between a logic "0" level and a logic "1" level to communicate the first value, the second value and the third value of the sensor 14 in serial fashion. Figure 3 illustrates the steps taken by the sensor 14 to report a sensed physical stimulus. Upon power up of the sensor 14, the state of the sensor is unknown. As such, the input signal 30 is held asserted to a logic level "0" at the input node 18 to force the sensor 14 to its initial or starting state. By forcing the sensor 14 to its starting state the content of the register 15 is reset. The sensor 14 remains in this state until the input signal 30 asserted at the input node 18 rises to a logic "1" level following at least one clock cycle of the clock signal asserted on the clock input node 24. Those skilled in the art will recognize that sensor 14 can be configured so that when the input signal 30 is asserted to a logic "1" level at the input node 18 to force the sensor 14 to its initial or starting state. Moreover, those skilled in the art will recognize that the input signal 30 can be asserted to a logic "0"

Please amend page 8, paragraph 3 to page 9 paragraph 1 as follows:

After one clock cycle on the clock input node 24, the sensor 14 shifts the measured value of the physical stimulus out of the register 15 on the output node 16 at a

rate of one bit per clock cycle on the clock input node 24 (step 56 in Figure 3). When the sensor has emptied the register 15, the sensor 14 affixes a [second] third data value to the response and asserts the [second] third data value on the output node 16 at the rate of one bit per clock cycle on the clock input node 24 (step 58 in Figure 3). The [second] third data value provides an indication that the sensor 14 is functioning correctly. As the output signal 32 illustrates, the affixed value corresponds to a 010 bit pattern. Nevertheless, those skilled in the art will recognize that the sensor 14 can affix an alternative bit pattern, such as 101 and the affixed value asserted by the sensor 14 can precede or follow the assertion of the measured value shifted out of the register 15. Moreover, those skilled in the art will recognize that the bit length of the measured response can vary depending on the application, the accuracy required and the like.

In the Claims:

Please amend Claims 1, 2, 3, and 8 as follows.

Please cancel Claims 4 and 5 without prejudice.

1. (Amended) A thermal sensor in an integrated circuit comprising:

a register to hold a response of said thermal sensor; and

an Input/Output (I/O) interface having an input node to receive an input trigger to trigger said thermal sensor to output on an output node of said interface an output signal that includes said response held by said register, [of said thermal sensor and to communicate] an indicator that indicates said thermal sensor is sensing the temperature of said integrated circuit, [followed by said response of said thermal sensor held by said register] and a value generated by said thermal sensor that indicates said thermal sensor is functioning properly.

2. (Amended) The thermal sensor of claim 1, wherein said Input/Output interface comprises a digital Input/Output interface having at least one input node capable of receiving a digital input and at least one output node capable of asserting a digital output.

3. (Amended) The thermal sensor of claim 2, wherein said [digital Input/Output interface] said input node and output node comprises at least two electrical contacts capable of providing an off chip interface.

8. (Amended) The thermal sensor of claim 1, wherein said thermal sensor appends said value that indicates said thermal sensor is functioning properly to said response of said thermal sensor.